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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/688,465	10/16/2000	Bernhard Schatzler	GR 97 P 1049 D	1415

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LERNER AND GREENBERG, PA
P O BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/688,465	Applicant(s) SCHATZLER ET AL.
	Examiner Nitin Parekh	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hara (US Pat. 5498902) in view of Lim et al. (US Pat. 5773878) and Reusch (US Pat. 4534105).

Regarding claim 1, Hara discloses an electronic component comprising:

- a flat pack/FP (6 in Fig. 11)
- a housing made of a casting/plastic molding/encapsulant (6 in Fig. 11)
- a lead frame (2/3/5 in Fig. 11) having an island/die pad with a continuous/unpatterned base area (2 in Fig. 11) supporting an integrated circuit (IC)/die (106 in Fig. 11)
- the IC/semiconductor element (1 in Fig. 11) being conventionally bonded/adhesively mounted (bonding adhesive not numerically referenced in

Fig. 11; Col. 1, line 23) to the island/die pad, the base area of the IC being smaller than that of the island/die pad, and

- the IC/die and the island/die pad being embedded in the housing so that a thickness of the housing region above the IC is substantially equal to that below the island/die pad (see Fig. 11)

(Fig. 11; Col. 1, lines 20-35).

Hara further teaches the outer leads extending in four directions such that the leads can have different orientation and shapes such as quad flat pack (QFP), plastic leaded chip carrier (PLCC), etc. (Col. 11, lines 43-54) and the packages being made thin and small to achieve the desired yield, function and application requirements (Col. 12, lines 12-40).

Hara fails to:

- explicitly teach in Fig. 11, the thickness of the housing region above the IC being substantially equal to that below the island/die pad, and
- teach the ratio between the base area of the IC and that of the island being 0.7-0.9 for avoiding the flexure of the housing.

Lim et al. teach using the thickness of a molding/housing region above the IC being substantially equal to that below the die pad/island (see X and Y in Fig. 4A) so that deformation/flexure of the package/housing can be prevented (Col. 3, lines 23-30).

Lim et al. further teach the die pad/island having a base area dimensions of 14 mm x 14 mm (Col. 1, line 35).

Reusch teaches a lead frame package having a chip support pad/island where a minimum clearance between the chip edge and the support pad/island is from 5-15 mils (0.125- 0.370 mm) to prevent the defects due to an adhesive overflow and to improve electrical performance (Col. 1, lines 10-35).

The above clearance dimensions from Reusch on length/width dimensions of Lim et al's die pad/island (14mmx14mm) yields base the base area/chip area being 189 sq. mm and 175 sq. mm for 5 mil and 15 mil clearance respectively, resulting in a ratio of the base area of the IC and that of the die pad/island being in a range of 0.96 to 0.89 respectively.

Furthermore, the determination/selection of the parameters such as the dimensions and respective range of the IC chip and die pad/island including width, thickness, shape, area/area ratio, resin thickness etc. in chip packaging and encapsulation is a subject of routine experimentation and optimization to achieve the desired support/rigidity and reduced stress, warpage and encapsulation related defects in the plastic package.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to arrive at a ratio between the base area of the IC and that of the island of 0.7- 0.9 for avoiding the flexure of the housing as taught by Lim et al. and Reusch so that the thermal stress and the overall size/weight of the package can be

reduced and a variety of die sizes can be accommodated in Hara's electronic component.

Regarding claim 2, Hara, Lim et al. and Reusch teach substantially the entire claimed structure as applied to claim 1 above, except a hollow groove formed on the IC by an amount of an adhesive emerged from between the IC and the island.

Lim et al. further teach an adhesive bonding (18 in Fig. 2) of the IC to the island (Col. 2, line 9) and a hollow groove shape/fillet being formed by emerged adhesive at the notch/groove/overhang portion of the island (see a corner/edge portion between 20 and 14 in Fig. 2).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the hollow groove being formed on the IC by the amount of an adhesive emerged from between the IC and the island as taught by Lim et al. so that the die bonding can be strengthened in Lim et al., Reusch and Hara's electronic component.

Regarding claim 3, Hara, Lim et al. and Reusch teach substantially the entire claimed structure as applied to claim 1 above, wherein Hara teaches the island/die pad (110 in Fig. 1) being a continuous/unpatterned area (see Fig. 11).

Regarding claim 4, Hara, Lim et al. and Reusch teach substantially the entire claimed structure as applied to claim 1 above, wherein Hara teaches conventional linking support/leads being routed to the island/die pad (see 35 in Fig. 3).

Regarding claim 5, Hara, Lim et al. and Reusch teach substantially the entire claimed structure as applied to claim 1 above, wherein Hara teaches the lead frame including the leads being vertically centered within the housing and the island/die pad being vertically lowered with respect to the leads (see 3 and 2 respectively in Fig. 11).

Response to Arguments

3. Applicant's arguments with respect to claims 1-5 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

NITIN PAREKH

PATENT EXAMINER

TECHNOLOGY CENTER 2800

05-10-04

NP